Modelsim do 脚本

# Testbench文件

\_tb.v文件，包括激励、实例化，结果显示。

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| --- |
| // Clk\_Chk\_tb.v  `timescale 1 ns/1ps  module Clk\_Chk\_tb;  reg rst\_n;  reg PHR;  reg PHR\_d;  reg PHR\_d1;  reg clk;  wire Err;  parameter clk\_period = 100; // clk period 10MHz = 100ns  parameter phr\_period = 66666667; // phr period 15Hz = 66 666 667  reg tbExpResult;  wire tbErr;  assign tbErr = Err;  // instance of Clk\_Chk  Clk\_Chk top\_inst(.rst\_n(rst\_n), .PHR(PHR), .PHR\_d(PHR\_d), .PHR\_d1(PHR\_d1), .clk(clk), .Err(Err));  // expected result  initial begin  tbExpResult = 1'b0;  end  // clock generator  always #(clk\_period/2) clk = ~clk;  initial begin  clk = 1'b0;  rst\_n = 1'b0;  PHR = 1'b1;  PHR\_d = 1'b1;  PHR\_d1 = 1'b1;  #(10\*clk\_period) rst\_n = 1'b1;  #(20\*clk\_period) forever #(phr\_period/2) PHR = ~PHR;  end  always@(posedge clk or negedge rst\_n)  begin  if(!rst\_n)  begin  PHR\_d <= 1'b1;  PHR\_d1 <= 1'b1;  end  else  begin  PHR\_d <= PHR;  PHR\_d1 <= PHR\_d;  end  end  // compare result  always@(posedge PHR) begin  if (tbErr != tbExpResult) begin  $display("Time %d ns, error!", $time);  end  else begin  //$display("ok!");  end  end  endmodule |

# Do脚本文件

do脚本文件使用的是tcl脚本，用tcl语言进行modelsim仿真的流程如下：

1. 建立库
2. 映射库到物理目录
3. 编译源代码
4. 启动仿真器
5. 执行仿真

vlib：建立库。格式vlib <library name>。库名缺省是work。

vmap：映射逻辑库名，将逻辑库名映射到库路径。语法vmap work <library name>。

vdir：显示指定库内容。语法vdir –lib <library name>

vlog：编译verilog源代码，库名缺省时编译到work，文件按顺序编译。语法vlog –work <library name> <file1>.v <file2>.v。编译vhdl源代码用vcom命令。

DO文件是ModelSim仿真的批处理文件，也就是tcl脚本文件。

Sim\_start.bat文件

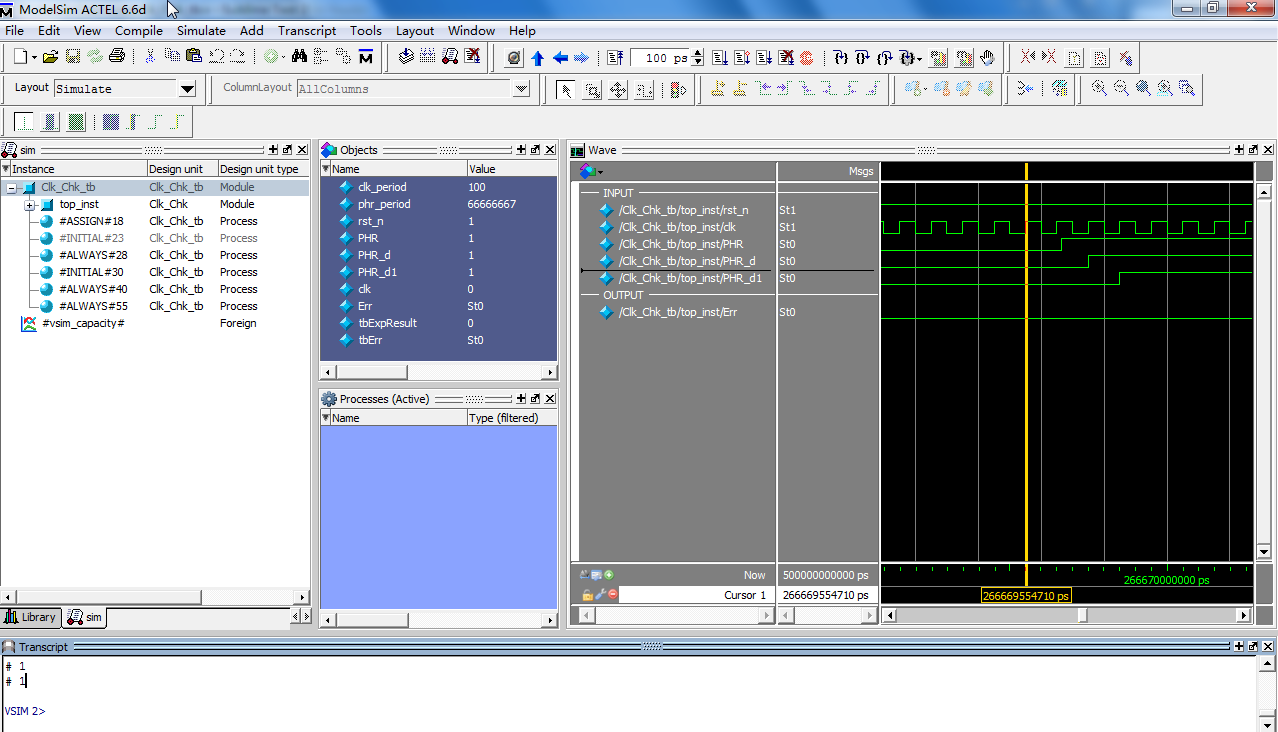
|  |
| --- |
| vsim -do Clk\_Chk\_sim.do |

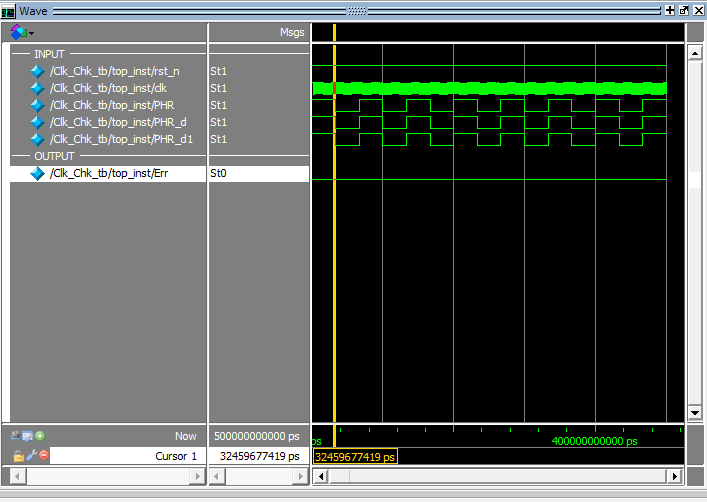
.do文件

|  |
| --- |
| # 创建库  vlib work  #映射库  vmap work work  #编译库的源文件到库  vlog -work work Clk\_Chk.v  vlog -work work Clk\_Chk\_tb.v  # 启动仿真  vsim \  -voptargs=+acc \  +transport\_int\_delays \  +transport\_path\_delays \  +notimingchecks \  -t ps \  -noglitch \  -multisource\_delay latest \  Clk\_Chk\_tb  set NumericStdNoWarnings 1  set StdArithNoWarnings 1  onbreak { resume }  # 添加信号到波形  do wave.do  run 500ms |

Wave.do文件

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| --- |
| # 如果有错误继续执行下一条命令而不停止  onerror { resume }  quietly WaveActivateNextPane {} 0  add wave -noupdate -divider INPUT  add wave -noupdate -format Logic /Clk\_Chk\_tb/top\_inst/rst\_n  add wave -noupdate -format Logic /Clk\_Chk\_tb/top\_inst/clk  add wave -noupdate -format Logic /Clk\_Chk\_tb/top\_inst/PHR  add wave -noupdate -format Logic /Clk\_Chk\_tb/top\_inst/PHR\_d  add wave -noupdate -format Logic /Clk\_Chk\_tb/top\_inst/PHR\_d1  add wave -noupdate -divider OUTPUT  add wave -noupdate -format Logic /Clk\_Chk\_tb/top\_inst/Err  TreeUpdate [SetDefaultTree]  # 设置光标位置  # WaveRestoreCursors {{Cursor 1} {2000 ns} 0},{{Cursor 2} {5000 ns} 0}  # 设置波形的属性  configure wave -namecolwidth 150  configure wave -valuecolwidth 100  configure wave -justifyvalue left  configure wave -signalnamewidth 0  configure wave -snapdistance 10  configure wave -datasetprefix 0  configure wave -rowmargin 4  configure wave -childrowmargin 2  configure wave -gridoffset 0  configure wave -gridperiod 1  configure wave -griddelta 40  configure wave -timeline 0  #更新配置  # update WaveRestoreZoom {0 ns} {100000 ns}  update |





# 附录

## Vsim命令的参数

-t <time\_unit>：指定仿真时间分辨率，单位可以是ps，ns，ms，sec，min，hr。如果用了verilog的`timescale指令，将使用这个设计中的最小时间精度；时间精度缺省是ns。

-sdfmin | -sdftype |-sdfmax <instance>=<sdf\_filename>：注释sdf文件，是可选项。

add wave /tb/ \*：该命令是将tb.v中模块tb下的所有信号加到波形文件中，注意\*前要加空格。

run <time\_step><time\_units>：执行命令，指定时间长度执行仿真。

-step：到下一个hdl状态

-continue：继续上次在-step或断点后的仿真。

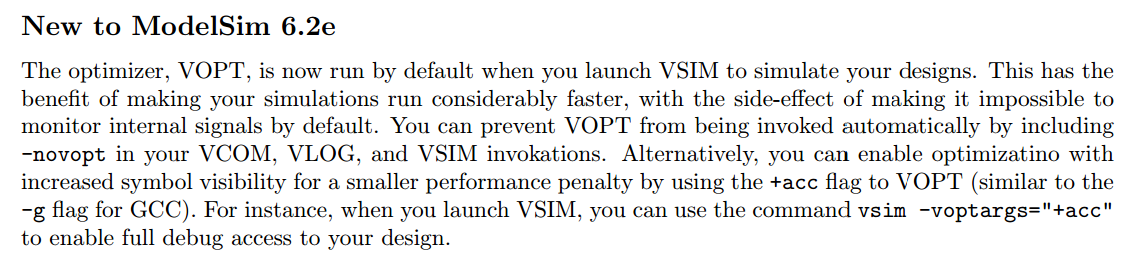
-all：一直运行。

-coverage

指定运行仿真时做仿真覆盖率计算，可选参数。

-voptargs=”+acc”

Enable full debug access to your design.



## Add wave命令

-format



## vsim命令大全

|  |
| --- |
| vsim -help  # Usage: vsim [options] [[<library>.]<primary>[(<secondary>)]]...  # -help Print this message  # -version Print the version of the simulator  # --------------------------- VHDL and Verilog options ---------------------------  # -assertdebug Keep data for debugging assertion failures  # -assertfile <filename> Alternative file for recording assert messages  # -errorfile <filename> Alternative file for recording error messages  # -assume Simulate PSL and Verilog assume directives same as assert directives  # -autoexclusionsdisable=fsm|assertions|all|none  # Turns on/off automatic fsm or assertions code coverage exclusions  # -c Command line mode  # -capacity Enable fine grain capacity analysis  # -coverage Allows enabled coverage statistics to be kept  # -do "<command>" Execute <command> on startup; <command> can be  # a macro filename  # -displaymsgmode <mode> Controls transcripting of display system task messages.  # Messages will appear in transcript and/or MsgViewer (.wlf file)  # Valid modes - tran, wlf, both (Default: tran)  # +dumpports+direction Provide port direction info in VCD file for dumpports  # +dumpports+unique Provide unique Extended VCD identifier for each port  # +dumpports+no\_strength\_range  # Ignore strength range when resolving conflicts  # +dumpports+collapse Collapse dumpport vectors into single VCD ids  # +dumpports+nocollapse Don't collapse dumpport vectors into single VCD ids  # +dumpports+force\_direction  # Ignore driver location. Use port direction for input and output ports  # -f <filename> Read command line arguments from <filename>  # -g<Name>=<Value> Specify generic/parameter default Value for Name  # -G<Name>=<Value> Override generic/parameter with specified Value  # -gui Open the GUI without loading a design  # -i Force interactive mode  # -keeploaded Prevent the simulator from unloading/reloading  # shared libraries  # -keeploadedrestart Prevent the simulator from unloading/reloading  # shared libraries during restart  # -keepstdout Do not redirect stdout to transcript window  # -l <filename> Write simulation log to <filename>  # (Default: transcript)  # -learn <fname> Learn the names of objects externally accessed at runtime  # (by methods such as PLI, VPI, SignalSpy, or CLI).  # <fname>.ocf, <fname>.ocm and <fname>.acc files created  # -lib <libname> Load top-level design units from <libname>  # (Default: work)  # -lic\_noqueue Do not wait in the license queue when a license  # is not available  # -lic\_vhdl Immediately reserve a VHDL license  # -lic\_vlog Immediately reserve a Verilog license  # -lic\_no\_viewer Disable checkout of viewer license and always use a  # simulation license to view  # -lic\_viewsim View with a simulation license if a viewer license  # is not available  # -memprof Collect memory allocation profile data for use with  # current simulation  # -memprof[+file=<filename>]  # Collect memory allocation profile data for use with  # current simulation and copy raw data to <filename>  # -memprof[+fileonly=<filename>]  # Collect memory allocation profile data in raw format  # to <filename>  # -modelsimini <modelsim.ini>  # Specify path to the modelsim.ini file  # -multisource\_delay min|max|latest  # Controls annotation of SDF INTERCONNECT construct  # (Default: max)  # +multisource\_int\_delays Enable multisource interconnect delays  # for both Verilog and VHDL  # -msgmode <mode> Controls transcripting of elaboration/runtime messages.  # Messages will appear in transcript and/or MsgViewer (.wlf file)  # Valid modes - tran, wlf, both (Default: both)  # +no\_notifier Disable notifier toggling for timing constraint  # violations  # -noassertdebug Do not keep data for debugging assertion failures  # -noassume Do not simulate PSL and Verilog assume directives  # -nocapacity Do not display capacity related information  # -noexcludehiz Do not automatically exclude rows with Hi-Z for  # expression coverage  # -nopsl Disable PSL assertions  # +no\_tchk\_msg Disable timing constraint error messages  # -note <msgNumber>[,<msgNumber>...] Change the severity of the listed  # messages to Note  # +notimingchecks Disable Verilog and VITAL timing checks  # -onfinish <mode> Customize the kernel shutdown behavior at the end of simulation  # Valid modes - ask, stop, exit, final (Default: ask)  # -pa Enable PowerAware RTL mode  # -pa\_lib <libname> Use PA specific dumps from <libname> library. (Default: work)  # -pa\_bboxprefix=<bbox\_prefix> Allow vsim to use different top level hierarchy for PA  # (Example: -pa\_bboxprefix=/tb2)  # -pedanticerrors Enforce strict language checks  # -permissive Relax some language error checks to warnings.  # -printsimstats Print simstats result at the end of simulation  # -psl Enable PSL assertions  # -psloneattempt Force single PSL assertion coverage attempt  # -pslinfinitythreshold Redefine infinite clock tick for strong operators  # -quiet Do not report 'Loading...' messages  # -runinit Execute run -init before command prompt or running -do files.  # -sdfmax[@<delayScale>] [<instance>=]<sdffile>  # Annotate VITAL or Verilog <instance> with maximum  # timing from <sdffile>, scaled by <delayScale>  # -sdfmaxerrors <n> Max number of missing instances reported (default is 5)  # -sdfmin[@<delayScale>] [<instance>=]<sdffile>  # Annotate VITAL or Verilog <instance> with minimum  # timing from <sdffile>, scaled by <delayScale>  # -sdfnoerror Treat SDF errors as warnings  # -sdfnowarn Disable warnings from SDF annotator  # -sdftyp[@<delayScale>] [<instance>=]<sdffile>  # Annotate VITAL or Verilog <instance> with typical  # timing from <sdffile>, scaled by <delayScale>  # +sdf\_verbose Display SDF annotator status messages  # -suppress <msgNumber>[,<msgNumber>...] Suppress the listed messages  # -t [1|10|100]fs|ps|ns|us|ms|sec Time resolution limit  # (VHDL default: resolution setting from .ini file)  # (Verilog default: minimum time\_precision in the  # design)  # -tag <string> Set tag for FLI/PLI tracing to <string>  # -notoggleints Excludes VHDL integers from toggle coverage  # -togglemaxintvalues Sets max number of values saved for VHDL integers  # -togglemaxrealvalues Sets max number of values saved for SystemVerilog reals  # -togglemaxfixedsizearray <size>  # Sets the limit on the size of Verilog unpacked fixed-size arrays  # that are included for toggle coverage  # -togglecountlimit Sets max count saved for a toggle node  # -togglewidthlimit Sets max width for vectors counted for toggles  # -togglevlogreal Includes Verilog real type in toggle coverage  # -togglefixedsizearray Includes Verilog unpacked fixed-size arrays, VHDL multi-d arrays and VHDL arrays-of-arrays in toggle coverage  # -togglevlogints Includes Verilog integers for toggle coverage  # -notogglevlogints Excludes Verilog integers from toggle coverage  # -notogglevlogreal Excludes Verilog real type in toggle coverage  # -notogglefixedsizearray Excludes Verilog unpacked fixed-size arrays, VHDL multi-d arrays and VHDL arrays-of-arrays in toggle coverage  # -togglepackedasvec Treat SystemVerilog packed structures and multi-d arrays as flattened vectors  # -togglevlogenumbits Treat SystemVerilog enums as reg-vectors for toggle coverage  # -extendedtogglemode [1|2|3]  # Change the level of support for extended toggles.  # The levels of support are:  # 1 - 0L->1H & 1H->0L & any one 'Z' transition (to/from 'Z')  # 2 - 0L->1H & 1H->0L & one transition to 'Z' & one transition from 'Z'  # 3 - 0L->1H & 1H->0L & all 'Z' transitions  # -title <string> Optional title for the Main window  # -trace\_foreign <n> Set FLI/PLI tracing to level <n>  # -unattemptedimmed Include immediate assertions to participate in assertion coverage calculations  # -vcdstim [<instance>=]<filename> Stimulate the top-level design or instances  # from an Extended VCD file  # -view [<dataset>=]<filename> View the contents of a WLF file  # -viewcov [<dataset>=]<ucdbfilename> View the contents of the coverage ucdb file  # -warning <msgNumber>[,<msgNumber>...] Change the severity of the listed  # messages to Warning  # -wlf <filename> Specify the name of the WLF file (Default: vsim.wlf)  # -wlfcompress Turn on WLF file compression (default)  # -wlfnocompress Turn off WLF file compression  # -wlfindex Turn on WLF file indexing (default)  # -wlfnoindex Turn off WLF file indexing  # -wlfopt Turn on WLF file optimization (default)  # -wlfnoopt Turn off WLF file optimization  # -wlfthreads Turn on WLF file threading (default if available)  # -wlfnothreads Turn off WLF file threading  # -wlflock Use WLF file locking (default)  # -wlfnolock Disable WLF file locking  # -wlfslim <size> Specify maximum number of Megabytes to be saved in  # WLF file (Default: infinite)  # -wlftlim <duration> Specify maximum duration of time to be saved in  # WLF file (Default: all)  # -wlfdeleteonquit Delete WLF file when simulation quits.  # -wlfnodeleteonquit Save WLF file when simulation quits. (default)  # -wlfcachesize Specify WLF reader cache size (per WLF file.)  # (Default: no reader cache)  # -wlfnocollapse Log every item event and preserve event order.  # -wlfcollapsedelta Log item values only at end of iteration. (default)  # -wlfcollapsetime Log item values only at end of time step.  # --------------------------------- VHDL options ---------------------------------  # -absentisempty Treat non-existent VHDL files opened for read  # as empty  # -nocollapse Disable optimization of internal port map connections  # -nofileshare Do not share file descriptors for VHDL files opened  # for write or append that have identical names  # -noglitch Disable VITAL glitch generation  # +no\_glitch\_msg Disable glitch error messages  # -std\_input <filename> Use filename for VHDL textio STD\_INPUT file  # -std\_output <filename> Use filename for VHDL textio STD\_OUTPUT file  # -strictvital Sacrifice performance for strict VITAL compliance  # -vital2.2b Select SDF mapping for VITAL 2.2b (Default: VITAL 95)  # -vital\_fix\_negative\_setup\_hold\_sum  # Set negative time to zero when setuphold sum is negative  # -------------------------------- Verilog options -------------------------------  # +alt\_path\_delays Use current output value instead of pending value  # when selecting inertial specify path output delay  # +bitblast[=[iopath|tcheck]] Bit-blast Verilog specify paths and/or tchecks with wide ports.  # Without the optional qualifiers operates on specify paths and tchecks.  # +bitblast=iopath bit-blasts specify paths with wide ports.  # +bitblast=tcheck bit-blasts tchecks with wide ports.  # -cvg63 Enforce 6.3 behavior of covergroups  # -cvgmaxrptrhscross Set the maximum cross bin BINRHS terms in coverage report.  # -cvgsingledefaultbin Collapse a Covergroup default array bin into a scalar bin  # -cvghaltillbin Halt simulation when an illegal cover/cross bin gets hit  # -cvgmergeinstances Set the default value of covergroup type\_option.merge\_instances to 1  # -cvgsparsecross Force modelling of Covergroup cross bins in a sparse fashion.  # -cvgsparsearraybin Force modelling of Covergroup unsize array bins in a sparse fashion.  # -nocrossautobins Avoid generating auto bins in cross coverage computation.  # -hazards Enable hazard checking  # +initmem+<seed> Specify seed value to be used for randomizing  # fixed-size arrays marked for randomization by vlog/vopt.  # +initreg+<seed> Specify seed value to be used for randomizing  # variables marked for randomization by vlog/vopt.  # +int\_delays Optimize annotation of interconnect delays  # -L <libname> Search library for design units instantiated from  # Verilog and for VHDL default component binding  # -Lf <libname> Same as -L, but libraries are searched before `uselib  # +maxdelays Use maximum timing from min:typ:max expressions  # +mindelays Use minimum timing from min:typ:max expressions  # +no\_cancelled\_e\_msg Disable negative pulse warning messages  # -noimmedca Revert to pre-6.5 continuous assignment event ordering  # +no\_neg\_tchk Set negative timing check limits to zero  # +no\_path\_edge Ignore the input edge specification on path delays  # +no\_pulse\_msg Disable path pulse error warning messages  # +nosdferror Treat SDF errors as warnings  # +nosdfwarn Disable warnings from SDF annotator  # +no\_show\_cancelled\_e Cancel negative pulse (Default)  # +nospecify Disable specify path delays and timing checks  # -nosva Disable SystemVerilog concurrent assertions  # -nocvg Disable Covergroup object construction and builtin calls  # -nocvg63 Enforce covergroup behavior as defined in SV IEEE-2009  # -nocvgmergeinstances Set the default value of covergroup type\_option.merge\_instances to 0  # +nowarn<CODE | Number> Disable specified warning message  # (Example: +nowarnTFMPC)  # +ntc\_warn Enable warnings from negative timing constraint  # algorithm  # -pli "<object list>" Load the list of PLI shared objects  # +<plusarg> Option accessible by PLI routine mc\_scan\_plusargs  # +pulse\_e/<percent> Set path pulse error limit as percentage of  # path delay  # +pulse\_e\_style\_ondetect Drive pulse error state immediately on detection  # +pulse\_e\_style\_onevent Drive pulse error state on time of pending event  # (Default)  # +pulse\_int\_e/<percent> Set interconnect pulse error limit as percentage  # of delay  # +pulse\_int\_r/<percent> Set interconnect pulse rejection limit as  # percentage of delay  # +pulse\_r/<percent> Set path pulse rejection limit as percentage of  # path delay  # +sdf\_nocheck\_celltype Disable check between SDF celltype name and  # module name  # +show\_cancelled\_e Drive pulse error state on negative pulse  # -solveengine <engine> Use specified solver engine to evaluate randomize() scenarios  # Valid engines - auto, bdd, act  # -solvefaildebug Display constraint conflicts on randomize() failure  # -solveflags=<flags> Modify constraint solver behavior for specific testcases  # (Example: -solveflags=ri)  # -solverev <version> Specify random sequence compatibility with <version>  # (Example: -solverev 6.2a)  # -sv\_seed <seed> Specify a seed for the Random Number Generator  # (RNG) of the root thread (SystemVerilog)  # -sva Enable SystemVerilog concurrent assertions  # -tab <filename> Specify PLI TAB file  # +transport\_int\_delays Use transport mode for interconnect delays  # +transport\_path\_delays Use transport mode for path delays  # (Default: inertial)  # +typdelays Use typical timing from min:typ:max expressions  # (Default)  # -v2k\_int\_delays Use Verilog 2000 style interconnect delays  # -wreal\_resolution <resolver>  # Specify resolve behavior for AMS wreal net  # with multiple drivers, where <resolver> is  # default, 4state, sum, avg, min, or max.  # -------------------------------- SystemC options -------------------------------  # -cpppath </path/to/[gcc|g++]>  # Specify path to the desired GNU compiler.  # Use same compiler path as specified on the sccom  # command line.  # -cppinstall <[gcc|g++] version>  # Specify the version of the desired GNU compiler  # supported and distributed by Mentor.  # Use same compiler path as specified on the sccom command line.  # -noautoldlibpath Disable setting of LD\_LIBRARY\_PATH set internally.  # -sc\_arg <arg> Specify a SystemC command line argument  # accessible using sc\_main(), sc\_argc() and  # sc\_argv()  # -scdpidebug Turn on debugging for SystemC DPI export function call  # -sclib <libname> Load the SystemC shared library from <libname>  # By default the systemc.so shared library is loaded  # from the library in which the top level SystemC design  # unit is compiled. This option should be used when systemc.so  # is not in the same library as the top level SystemC design unit. |